PRODUCT SPECIFICATION FOR LCD MODULE

Revision: 0.0

Model No: T15P00

Module Type: COG+FPC+BL

APPROVED SIGNATURE

□ Approved Product Specification only
■ Approved Product Specification and Samples

Prepared By	Checked By	Approved By

Contents

1. General Description

T15P00 is a transmissive type a-Si TFT-LCD (amorphous silicon thin film transistor liquid crystal display) module, which is composed of a TFT-LCD panel, a driver circuit and a backlight unit. The panel size is 1.5 inch and the resolution is 480*240, the panel can display up to 16.7M colors.

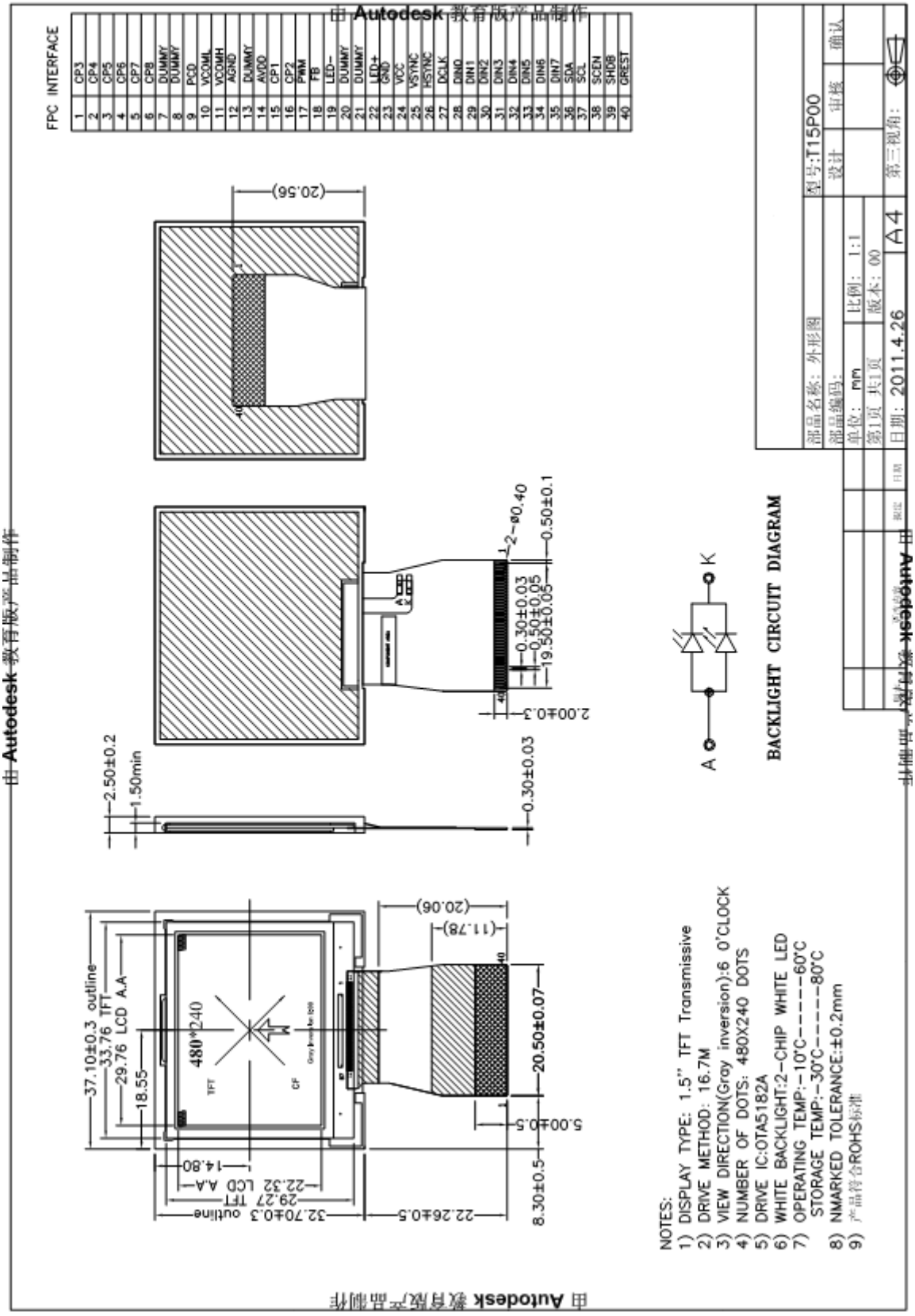
2. Physical Features

Display Mode	TFT-LCD Module
	Active matrix TFT, Transmissive type
Display Format	Graphic 480×240 Dot-matrix
Input Data	8bit RGB interface
Viewing Direction	6 O'clock
Driver IC	OTA5182A

3. Mechanical Specification

Item	Contents	Unit
Module size (W×H×T)	37.10 × 32.70× 2.50	mm
Number of dots	480×240	---
Active area (W×H)	29.76×22.32	mm

4. Outline Dimension



5. Absolute Maximum Ratings

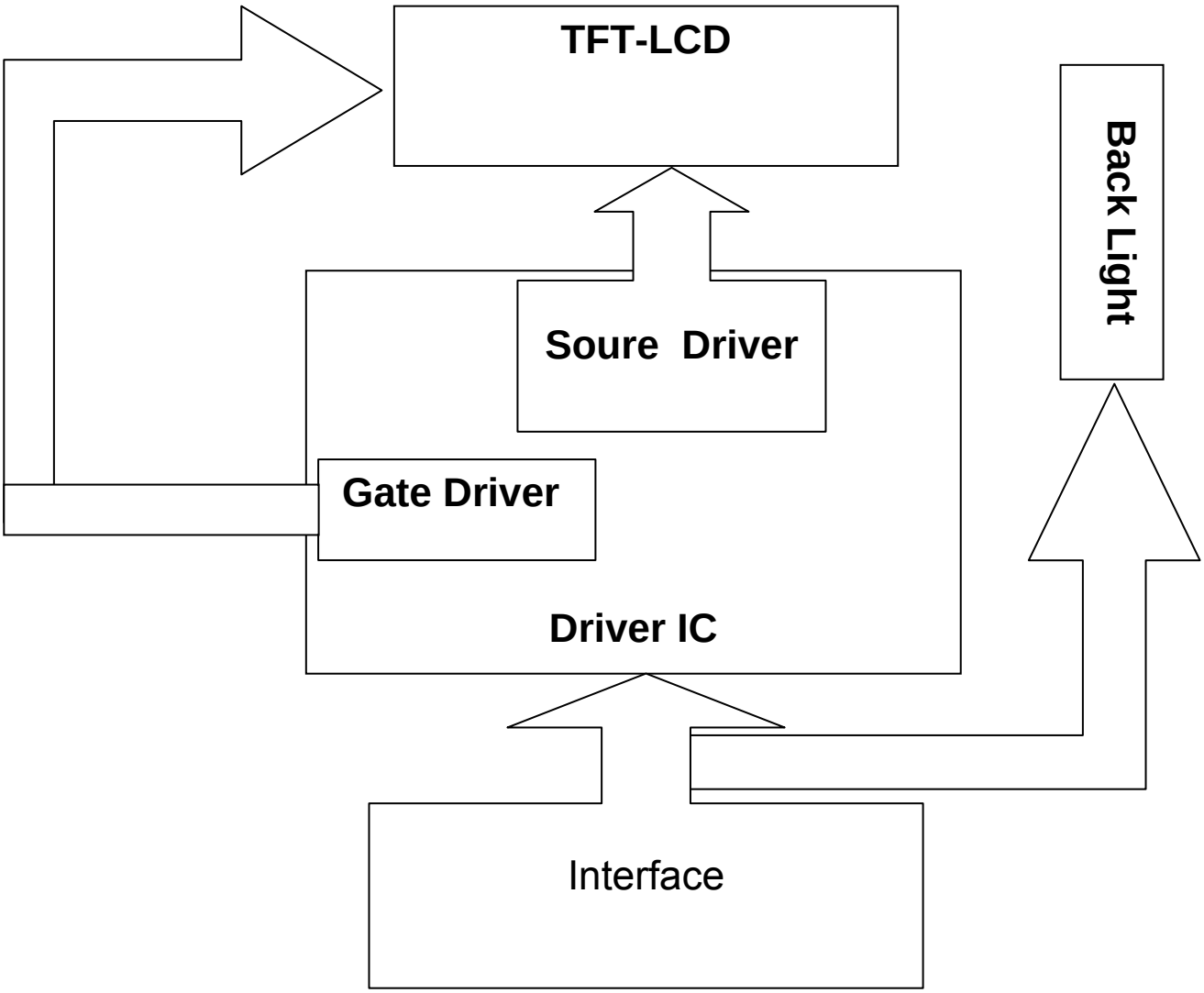
Item	Symbol	Min	Max	Unit
supply voltage	VCC	-0.5	6	V
Operating temperature	TOPR	-10	60	℃
Storage temperature	TSTR	-30	80	℃

6. Electrical Characteristics

Item		Symbol	Rating			Unit	Remark
			Min	Typ	Max		
Power Voltage		VCC	3.0	3.3	3.6	V	---
Input Voltage	L level	VIL	GND	---	0.3*VCC	V	---
	H level	VIH	0.7*VCC	---	VCC	V	
LCD Drive Power Consumption		Wp	---	25	---	mW	---

7. Module Function Description

7-1. Block Diagram Of LCM



7-2. Pin Description

PIN NO.	Symbol	Description
1	CP3 (VDD_25V)	Capacitor for power setting and need to connect a capacitor(1.0 uF/10V) to GND.
2	CP4 (VDD3)	Intermediate voltage for charge pump and need to connect a capacitor((1.0 uF/16V) to GND.
3	CP5	DUMMY
4	CP6	DUMMY
5	CP7	DUMMY
6	CP8	DUMMY
7	DUMMY	DUMMY
8	DUMMY	DUMMY
9	PCD	DUMMY
10	VCOML	DUMMY
11	VCOMH	DUMMY
12	AGND	Anolog ground.
13	DUMMY	DUMMY
14	AVDD (VCAC)	Defines the amplitude of the VCOM swing and need to connect a capacitor(1.0 uF/10V) to GND.
15	CP1 (FRP)	Frame polarity output and need to connect a capacitor(1.0uF/10V) to CP2.
16	CP2 (VCOM)	Vcom and need to connect a capacitor(1.0uF/10V) to CP1.
17	PWM (DRV)	Gate signal for the power transistor of theboost converter.
18	FB	Main boost regulator feedback input.
19	LED-	Backlight input

20	DUMMY	DUMMY
21	DUMMY	DUMMY
22	LED+	Backlight input
23	GND	Digital ground
24	VCC	Power supply
25	VSYNC	Vertical sync input
26	HSYNC	Horizontal sync input
27	DCLK	Clock signal
28—35	DIN0—DIN7	Data bus
36	SDA	Serial data input
37	SCL	Serial clock input
38	SCEN	Serial chip select
39	SHDB	Standy mode
40	GREST	Global reset pin

7-3. Timing Characteristics

7-3-1 Input Data Format

RAW DATA MODE

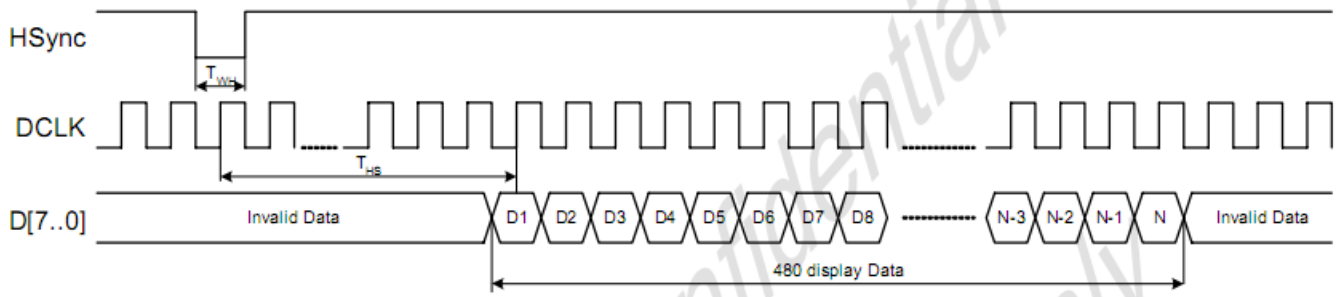


Figure 9: RAW DATA MODE data input format

SERIAL MODE 24.54MHz

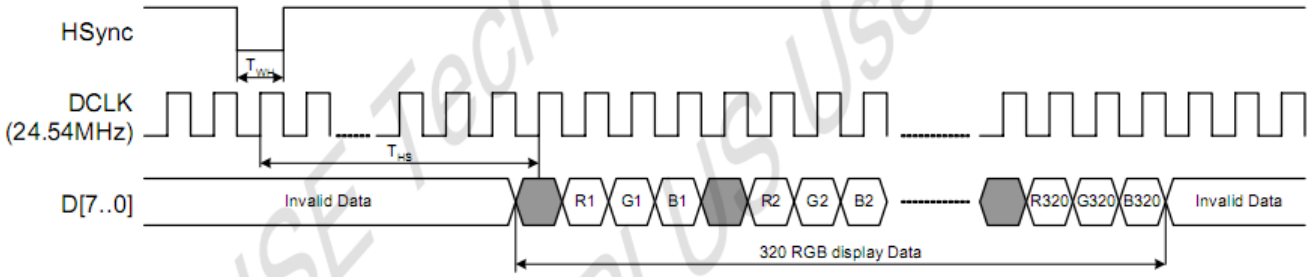


Figure 10: SERIAL MODE 24.54MHz Data input format (Sel=001)

SERIAL MODE 27MHz

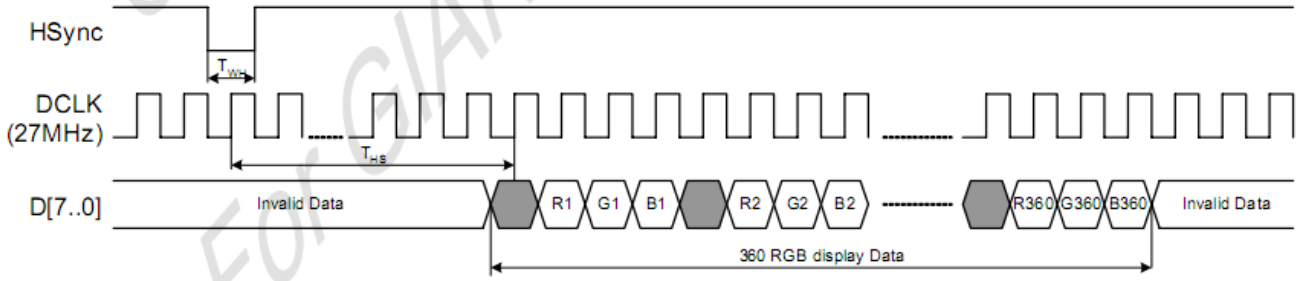


Figure 11: SERIAL MODE 27MHz Data input format (Sel=010)

CCIR656

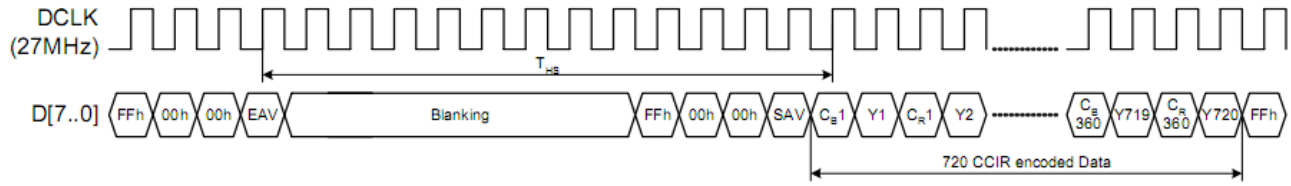


Figure 12: CCIR Data input format

7-3-2 Vertical input timing

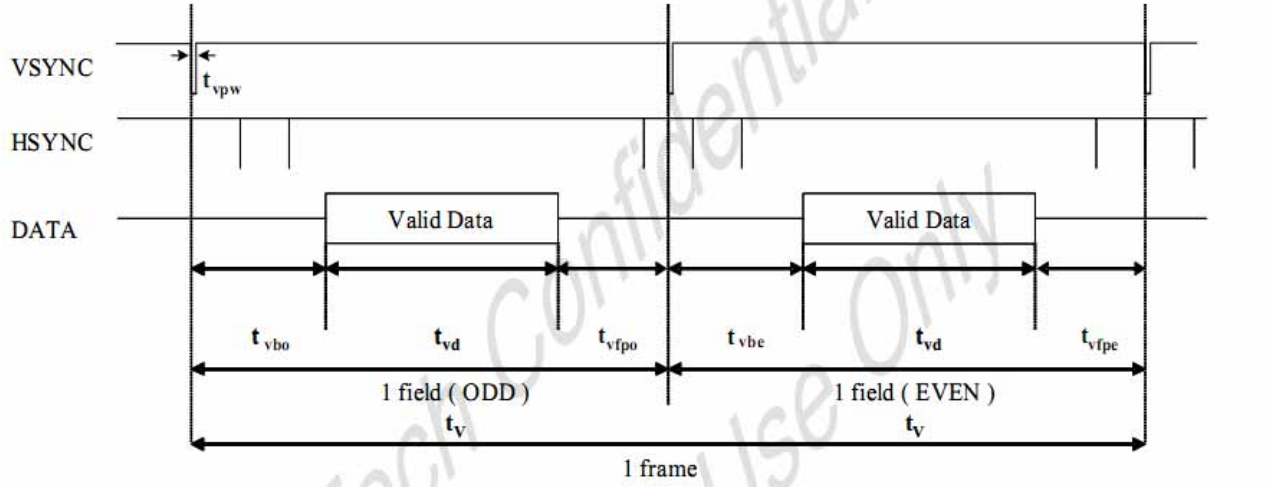


Figure 13: Vertical input timing diagram for interlace application

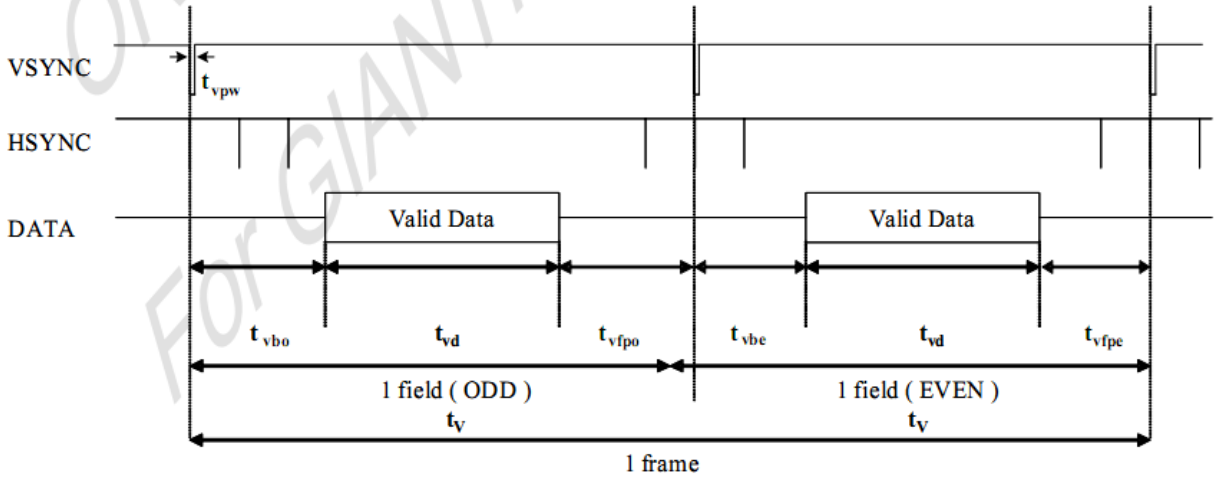


Figure 14: Vertical input timing diagram for non-interlace application

Raw data vertical input timing

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

Serial RGB vertical input timing

NTSC

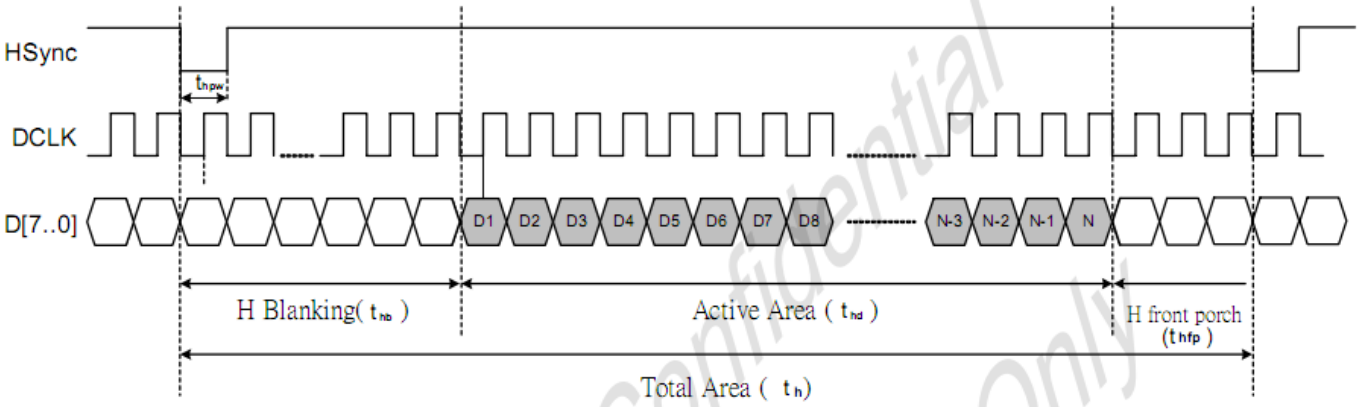
Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

PAL

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		288(280)			288(280)		H
VSYNC period time		t_v	295.5 (287.5)	312.5	325.5 (317.5)	295 (287)	312	325 (317)	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	11.5(19.5)	16.5	1	11(19)	16	H
	Even field	t_{vfpe}	1	11(19)	16				

(*) Non-interlace mode: NTSC is 262 lines (typical), but 263 is tolerant.
PAL is 312 lines (typical), but 313 is tolerant.

7-3-3 Horizontal input timing



RAW Data

Parameter		Symbol	Value			Unit
Horizontal display area		t_{hd}	480			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	
			8.1	9.7	11.3	Mhz
1 Horizontal Line		t_h	617			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			
	Typ.		1			
	Max.		96			
HSYNC blanking		t_{hb}	84	100	115	
HSYNC front porch		t_{hfp}	53	37	22	

SERIAL RGB MODE

NTSC

Parameter		Symbol	Value			Value			Value			Unit
Horizontal display area		t_{hd}	1280			1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max	
			20.47	24.54	28.66	22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1560			1716			1716			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			1			
	Typ.		1			1			1			
	Max.		96			96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	43	28	12	71	56	40	39	24	8	

PAL

Parameter		Symbol	Value			Value			Unit
Horizontal display area		t_{hd}	1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	
			22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1728			1728			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			
	Typ.		1			1			
	Max.		96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	83	68	52	51	36	20	

CCIR

PAL

Parameter		Symbol	Value			Value			Unit
Horizontal display area		t_{hd}	1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	
			22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1728			1728			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			
	Typ.		1			1			
	Max.		96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	83	68	52	51	36	20	

7-3-4 SPI Timing

There is a total of 16 registers each containing several parameters. For a detailed description of the parameters refer to Table 1.

The serial register has read/write function. D[15:12] are the register address, D[11] defined the read or write mode and D[10:0] are the data.

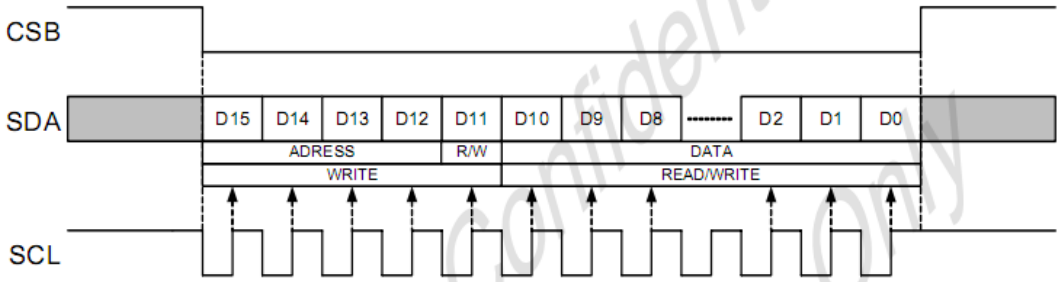


Figure 2: Serial Interface read/write sequence

At power-on, the default values specified for each parameter (in Table 1) are taken.

All data, except S0 D[3:2], are validated on the negative edge of Vsync.

In 3-wire register, GRB clear registers to default value except GRB value.

If less than 16-bit data are read during the CS low time period the data is cancelled.

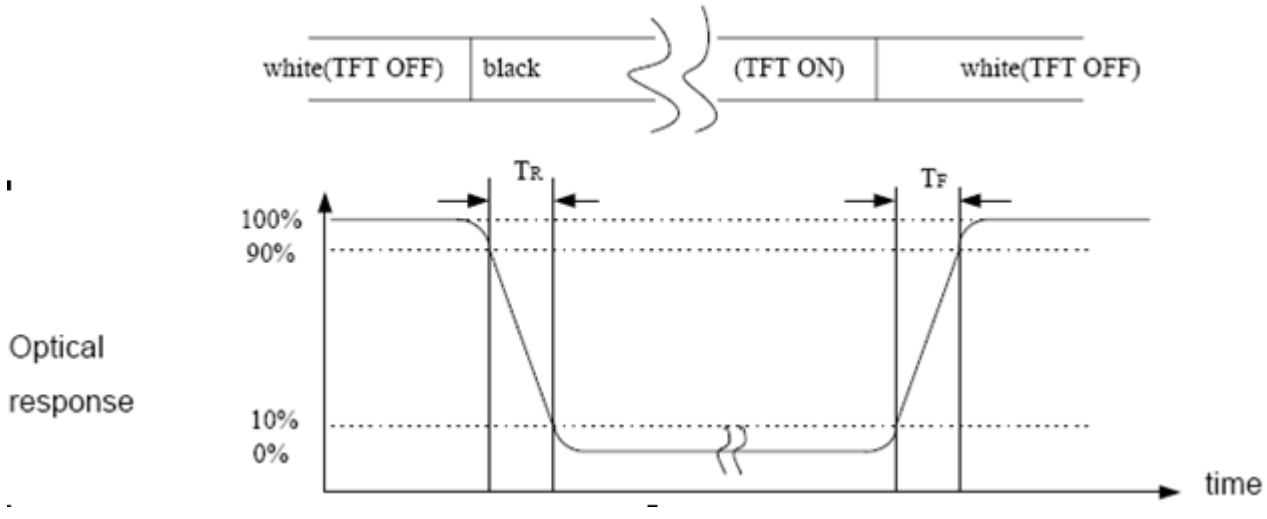
Serial communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		240			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

8. Electro-Optical Characteristics(only for TFT panel reference)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr +Tf	θx = θy =0	---	25	---	ms	Note 1
Contrast Ratio		CR		---	300	---	---	Note 2
Transmittance (without Polarizer)		T%		---	13	---	%	
Color chromaticity	white	Wx		---	0.303	---	-	Reference Only
		Wy		---	0.339	---		
	Red	Rx		0.565	0.585	0.605		
		Ry		0.319	0.339	0.359		
	Green	Gx		0.284	0.304	0.324		
		Gy		0.511	0.531	0.553		
	Blue	Bx		0.122	0.142	0.162		
		By		0.145	0.165	0.185		
Viewing angle	θ_{21}		CR ≥ 10	---	20	---	Deg.	Note 3
	θ_{22}			---	50	---		
	θ_{12}			---	40	---		
	θ_{11}			---	40	---		
Module Luminance ($I_F = 40mA$)		L			250	---	cd/m2	Note4

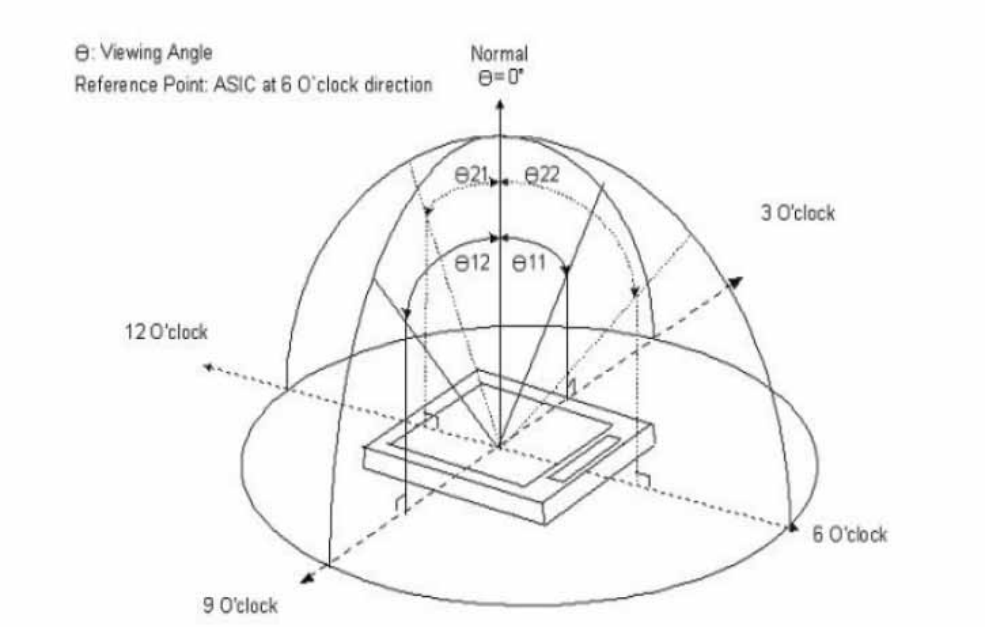
Note(1) Definition of Response Time:Sum of T_R and T_F



Note (2) Definition of Contrast Ratio(CR):measureed at the center point of panel

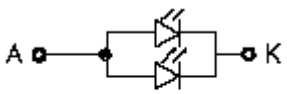
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Viewing Angle θ and ϕ:



Note(4)

a. Test Instrument:BM-7(Distance:500mm;Field=1°)
b. Light Source: LED*2(White)



CIRCUIT DIAGRAM

c. Conditions: $I_F = 40mA$, $V_{BL} = 3.2V$
d. Uniformity=(Min. Brightness/ Max. Brightness)*100%
e. Uniformity $\geq 80\%$

9. Reliability

Test Condition:

No.	ITEM	CONDITION	CRITERION
1	High Temperature Non-Operating Test	80℃ * 240Hrs	1.No Defect Of Operational Function In Room Temperature Are Allowable. 2.IDD of LCM in Pre-and Post-Test Should Folllow Specification
2	Low Temperature Non-Operating Test	-30℃ * 240Hrs	
3	High Temperature/Humidity Non-Operating Test	50℃ * 90%RH * 240Hrs	
4	High Temperature Operating Test	60℃ * 240Hrs	
5	Low Temperature Operating Test	-20℃ * 240Hrs	
6	Thermal Shock Test	-20℃(30 Min)↔60℃(30Min)*10 Cycles	

10. Inspection Standards

1. AQL(Acceptable Quality Level)

AQL of major and minor defect

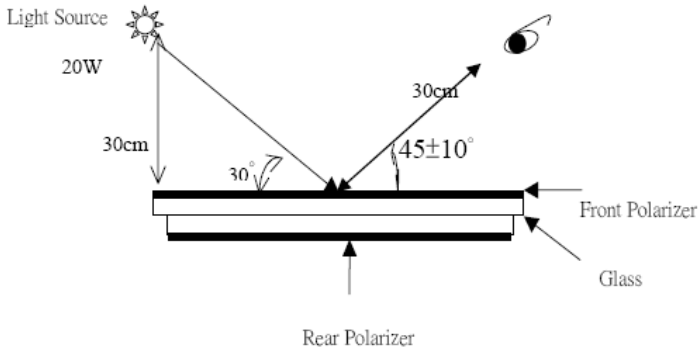
	MAJOR DEFECT	MINOR DEFECT	MAJOR+MINOR
APPEARANCE	0.40%	1.0%	1.0%
ELECTRIC-OPTICAL	0.15%	0.15%	0.15%

2. Basic conditions for inspection

The LCM face to us, in normal environment, the lux is 1000±200.(Darkroom's lux:100±50),

About an angle of incidence 30, a distance of 30cm with normal eye,with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

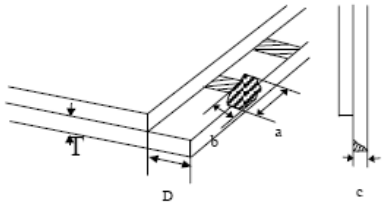
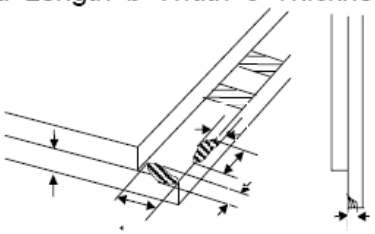


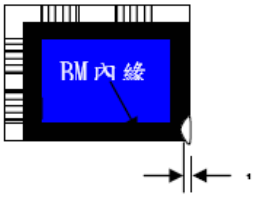
3. Inspection item and criteria

3.1 Visual inspection criterion in immobility

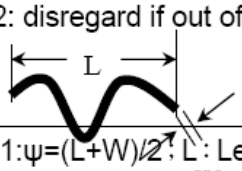
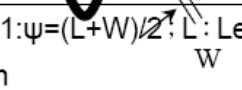
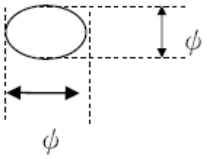
3.1.1 Glass defect

No	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	

No	Defect item	Criteria	Remark
2	Cracks (Major defect)	1.Linear cracks on panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage 1) b≦1/3Pin width(non bonding area) 【Accept】 2) bonding area≦0.5mm 【Accept】	a:Length, b:Width
4	Pin-side，conductive area damaged (minor defect)	(a c：disregards) b≦ 1/3 of effective length for bonding electrode 【Accept】	a：Length，b：Width，c：Thickness 
5	Pin-side，non-conductive area damaged (minor defect)	1) Damage area don't touch the ITO (Inclueling contraposition mark,except scribing mark) 【Accept】 2) c<T b≦BM 1/3 of width 【Accept】 3) c=T b not touch the seal glue 【Accept】 4) a disregards	a：Length，b：Width，c：Thickness 

No	Defect item	Criteria	Remark
6	Non-pin-side damage (minor defect)	c<T 1) b exceeds 1/3 BM 【Reject】 c=T b not touch the seal glue 【Reject】	c : Thickness b: width of damage 

3.1.2 LCD appearance defect (View area)

No	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1: L：Length，W：Width note2: disregard if out of AA 
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	
2	Polarizer bubble、concave and convex (minor defect)	ψ≦0.2mm	disregard	note 1:ψ=(L+W)/2；L：Length，W：Width note2: disregard if out of AA 
		0.2mm<ψ ≦ 0.3mm	2	
		0.3mm<ψ ≦ 0.5mm	1	
		0.5mm<ψ	0	
3	Black dots、dirty dots、impurities、eyewinker (Major defect)	ψ≦0.15mm	disregard	note2: disregard if out of AA 
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
4	Polarizer prick (Major defect)	ψ≦0.1mm	disregard	note1:ψ=(L+W)/2 ；L= Length，W=Width note2: the distance between two dots ＞5mm
		0.1mm<ψ≦0.25mm	3	
		ψ＞0.25mm	0	

3.1.3 .FPC

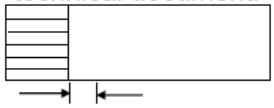
No	Defect item	Criteria		Remark
1	Copper screen peel (Major defect)	Copper screen peel 【Reject】		
2	No release tape or peel (Major defect)	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	note1: Cannot have stride ITO impurities
		ψ≦0.25mm	2	
		ψ>0.25	0	

3.1.4 Black tape & Mara tape

1	FPC or H/S black tape shift (minor defect)	1.shift spec: 1)glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1) exceed of FPC edge or H-S edge 【Reject】 2)IC bare 【Reject】	
2	No black tape (Major defect)	No black tape 【Reject】	
3	Tape position mistake (minor defect)	Not by engineering drawing 【Reject】	
4	Mara tape defect (minor defect)	Peel before pulling the protecting film. 【Reject】	

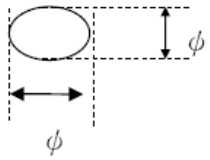
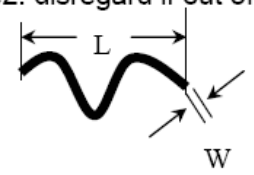
3.1.5 Silicon and Tuffy glue

No	Defect item	Criteria	Remark
1	Quantity of silicon (minor defect)	Uncover the ITO and circuit area. 【Reject】	note: compared by engineering drawing.

No	Defect item	Criteria	Remark
2	Tuffy glue (minor defect)	1. Uncover the reveal copper area 【Reject】 2. Cover layer 0.3mm(Min) ~ 3.0mm(Max) 【accept】	note:if customer has special requirement , refer to the technical document. 
3	Depth of glue covering (minor defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement。

3.2 Electrical criteria

No	Defect item	Criteria	Remark
1	No display (Major defect)	No display 【Reject】	
2	Missing line (Major defect)	Missing line 【Reject】	
3	Seg-com light and dark (Major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (Major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (Major defect)	Flicker of Pattern 【Reject】	
6	Mura (Major defect)	ND filter 2% test	
7	Over current (Major defect)	Over current 【Reject】	
8	Voltage out of specification (Major defect)	Voltage out of specification 【Reject】	
9	Pattern blur ,error code (Major defect)	Pattern blur ,error code 【Reject】	
10	Dark light, Flicker (Major defect)	Dark light, Flicker 【Reject】	

No	Defect item	Criteria	Remark	
11	Black/White dots 、Dirty dots、eyewinker (Major defect)	Specification	Allowable	Note1: disregard if out of AA 
		ψ≦0.15mm	disregard	
		0.15mm<ψ ≦ 0.25mm	2	
		0.25mm<ψ ≦ 0.3mm	1	
		0.3mm<ψ	0	
12	Fiber、glass cratch、polarizer scratch/folded (minor defect)	W≦0.03mm	disregard	note1: L : Length、W : Width note2: disregard if out of AA 
		0.03mm<W≦0.05mm ; L≦3.0mm	2	
		0.05mm<W≦0.1mm; L≦3.0mm	1	
		W>0.1mm ; L>3.0mm	0	

11. Precautions For Using LCD Modules

Please pay attentions to the followings as using the LCD module.

11. 1 Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the ITO film very fragile and easy to be damaged, do not hit, press or rub the display surface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Wipe off water droplets or oil immediately.

(f) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(g) Do not touch the output pins directly with bare hands.

(h) Do not disassemble the LCD module.

11. 2 Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

11. 3 Operation

(a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI and electronic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

11. 4 Others

(a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

(b) It is recommended to peel off the protection film on the ITO film slowly so that the electrostatic charge can be minimized.

(c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge can be minimized.

12. Records Of Version

Version	Revise Date	Page	Content
0.0	2011-05-10	All	New released